THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today
(1) was not written for publication in a law journal and
(2) is not binding precedent of the Board.

Paper No. 33

UNITED STATES PATENT AND TRADEMARK OFFICE

_____

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

_____

Ex parte HIROKAZU EZAWA, MASAHIRO MIYATA

_____

Appeal No. 1997-0166
Application No. 08/409,933

_____

ON BRIEF

_____

Before HAIRSTON, FLEMING and LEVY, **Administrative Patent Judges**.

LEVY, **Administrative Patent Judge**.

DECISION ON APPEAL

This is a decision on appeal from the examiner's final rejection of claims 8, 9, and 11-28, which are all of the claims currently pending in this application.

BACKGROUND

The appellants' invention relates to a semiconductor device having a protruding bump electrode. Specifically, a bump electrode (5a) is positioned above a semiconductor substrate (1). An electrode pad (2a) and a metal layer (4a) are located between the bump electrode and substrate to allow signals to be input and output to and from the semiconductor device. A resin film (6) covers a surface of the substrate. The bump electrode is disposed in an opening (fig. 4) in the resin film and projects a distance (fig. 7) above a top surface (8) of the resin film. An understanding of the invention can be derived from a reading of exemplary claim 17, which is reproduced as follows:

> 17. A semiconductor device comprising: a semiconductor substrate;
>
> at least one bump electrode positioned above the semiconductor substrate, the bump electrode and semiconductor substrate having an electrode pad and metal layer therebetween to allow signals to be input and output to and from the semiconductor device; and
>
> a resin film covering a surface of the semiconductor substrate, the resin film having an opening positioned above the electrode pad, the bump electrode being disposed in the opening of the resin film and projecting a distance above a top surface of the resin film, said projection distance reducing heat induced defects and absorbing pressure exerted on a top area of the bump electrode to suppress occurrence of cracks in the resin film.

The prior art references of record relied upon by the examiner in rejecting the appealed claims are:

Merrin et al. (Merrin)	3,436,818	Apr. 08, 1969
Engeler et al. (Engeler)	3,714,520	Jan. 30, 1973

Yabe JP 62-232147 Oct. 12, 1987

Claims 8, 9, and 11-28 stand rejected under 35 U.S.C. § 103 as being unpatentable over Yabe in view of Merrin and Engeler.

Rather than reiterate the conflicting viewpoints advanced by the examiner and the appellants regarding the above-noted rejection, we make reference to the examiner's answer (Paper No. 23, mailed June 26, 1996) for the examiner's complete reasoning in support of the rejections, and to appellants' brief (Paper No. 21, filed June 14, 1996) and reply brief (Paper No. 25, filed August 22, 1996) for appellants' arguments thereagainst.

We note that the examiner's answer contains a new ground of rejection. Appellants filed an amendment in response to the new ground of rejection (Paper No. 24, filed August 22, 1996). In an advisory action (Paper No. 26, mailed October 25, 1996) and an interview summary (Paper No. 35, mailed May 18, 1999) the examiner noted that the amendment filed on August 22, 1996 has been entered. A copy of the claims on appeal is found as an appendix to appellants' reply brief.

OPINION

In reaching our decision in this appeal, we have given careful consideration to appellants' specification and claims, to the applied prior art references, and to the respective positions articulated by the appellants and the examiner. As a consequence of our review, we make the determinations which follow.

Appellants state (brief, page 5) that claims 8, 9 and 11-28 do not stand or fall together and that appellants "have set forth reasons supporting the separate patentability of the claims." We note, however, that claims 8, 11-13, 18, 22 and 27 have not been separately argued. 37 CFR § 1.192 (c) (7) (July 1, 1996) ***as amended at*** 60 Fed. Reg. 14518 (March 17, 1995), which was controlling at the time of appellants' filing of the brief, states:

> For each ground of rejection which appellant contests and which applies to a group of two or more claims, the Board shall select a single claim from the group and shall decide the appeal as to the ground of rejection on the basis of that claim alone unless a statement is included that the claims of the group do not stand or fall together and, in the argument under paragraph (c) (8) of this section, appellant explains why the claims of the group are believed to be separately patentable. Merely pointing out differences in what the claims cover is not an argument as to why the claims are separately patentable.

Accordingly, we will consider appellants' claims 8, 11-13, 18, 22 and 27 as standing or falling with the claims from which they depend.

We will affirm the rejection of claims 8, 9, 17-19, and 21-23 under 35 U.S.C. § 103. We will reverse the rejection of claims 11-16, 20 and 24-28 under 35 U.S.C. § 103.

Turning first to independent claims 17 and 21, we note that the claims are similar in scope, with claim 21 additionally setting forth that the electrode pad is disposed on a surface of the semiconductor substrate. Appellants assert (reply brief, page 6) that the references do not disclose or suggest the electrode pad recited in the claims. It is the examiner's position (answer, pages 3 and 5) that figure 1 of Yabe discloses an electrode pad, and that even though the pad is not labeled, it would

have been clear to one of ordinary skill and knowledge of the art that the element under the bump electrode is indeed a pad as it is a configuration that is fundamental in the semiconductor art. Appellants argue that it is evident from review of the translation of Yabe, supplied by appellants with an amendment filed on October 2, 1995, that Yabe does not show or describe an electrode pad between the bump electrode and the substrate. From our review of Yabe, we note that figures 1 and 2 show a structure between insulating layer (3) and the lower portion of bump electrode (4). However, it is unclear from the drawing of Yabe as to whether or not this structure is an electrode pad. Turning to the specification of Yabe, the specification is silent as to this structure. As the structure shown in the drawing is between the bump electrode and the insulating layer of the semiconductor chip, we find that the structure disclosed by Yabe is an electrode pad. However, if we are incorrect as to the structure of Yabe being an electrode pad, then we find that the secondary reference to Merrin clearly teaches this feature, for the reasons set forth, ***infra***. Appellants assert (reply brief, page 6) that Merrin does not supply the deficiencies of Yabe because in Merrin, the aluminum land (18) is formed on chip (15) rather than on substrate (11). Additionally, appellants argue (reply brief, page 7) that the aluminum land is positioned between the chip (15) and the mound (24), rather than between the substrate (11) and the mound (24) and that (reply brief, page 5) "[b]ecause Merrin specifically discloses that the chip 15 is a resistor, transistor, or diode, there would not be a reason to assume that the chip 15 includes a <u>semiconductor</u> substrate." Claims 17 and 21 call for an

electrode pad between the semiconductor substrate and the bump electrode. Merrin is directed to a process for providing an interconnection between the terminal areas of active microminiaturized chip devices such as transistors and/or diodes to connecting areas of a conductive pattern on a supporting dielectric substrate while providing standoff between the pattern and chip device (col. 1, lines 28-48 and col. 7, lines 19-25). We find aluminum land (18) of Merrin to be disposed on a semiconductor substrate and to be located between a semiconductor substrate and mound (24) because Merrin discloses that the microminiaturized devices may be diodes and transistors which are active devices or "chips" and further states (col. 4, line 73 through col. 5, line 1) that "[d]uring the fabrication of chip 15 (Step 17) an aluminum land 18 (FIGURE 3) is deposited on each semiconductor region to provide the desired ohmic contact" [emphasis added]. As chip (15) includes a semiconductor region where the aluminum land (18) is deposited, we find that aluminum land (18) is located on a semiconductor substrate, as claimed. Accordingly, we therefore also find that Merrin teaches placement of the aluminum land (18) between the semiconductor substrate of chip (15) and mound (24). We conclude that it would have been obvious to one of ordinary skill in the art to have provided the bump electrode (4) of Yabe with an electrode pad between[1] the silicon chip (1) and the bump electrode (4) in view of the teachings of Merrin.

[1] We note that page 6 of appellants' specification states the appellants' electrodes "are formed, in actual practice, over the substrate 1 with an insulating film provided therebetween," and that Yabe shows similar layers (1) and (3).

Appellants further assert that the references do not disclose or suggest the metal layer recited in claims 17 and 21. It is the examiner's position that Merrin discloses the use of a metal layer (figures 4 and 5) and that (answer, page 4) it would have been obvious to one of ordinary skill in the art to have inserted a metal layer between an electrode pad and an electrode bump to facilitate the transference of electrical signals to and from a semiconductor device. Appellants' position (reply brief, page 5) is that in Merrin, the chromium layer (21) is positioned between the chip (15) and the solder mound (24) rather than between the solder mound (24) and the substrate (11). At the outset, we note, as stated ***supra***, that we find the chip (15) to include a semiconductor substrate in view of Merrin's disclosure that the microminiaturized devices may be diodes and transistors which are active devices or "chips," and that (col. 4, line 73 through col. 5, line 1) "[d]uring the fabrication of chip 15 (step 17) an aluminum land 18 (FIGURE 3) is deposited on each semiconductor region." Accordingly, we find that in Merrin, the chromium layer (21) with copper (22) and gold (23) deposits, is located between the solder mound (24) and a semiconductor substrate of chip (15). With respect to the issue of whether it would have been obvious to have provided the bump electrode of Yabe with a metal layer as taught by Merrin, we first turn toYabe, who recognizes (translation, page 3) that a problem in the prior art is that the surface protective layer (5) is polyimide which suffers from the drawback of lacking moisture resistance. To overcome this problem, Yabe adds SiO_2 powder to the polyimide film around the bump electrode and at a thickness of 2 *u*m and states (translation, page 4) that "[t]he effect of having a polyimide film with

added SiO_2 around the bump is that shorting between the TAB lead and the chip end is avoided, and circuits in the chip can be protected with favorable moisture resistance." The remainder of the silicon chip (1) of Yabe is covered with a film (3) of silicon nitride or SiO_2. We now turn to Merrin, who discloses (col, 5, lines 1 through 15) that subsequent to the application of the aluminum lands (18), a layer of glass (19) is deposited over the chip (15) to provide environmental protection. Holes are then etched in the glass (19) over the lands to expose them for metallization. Layers of chromium (21), copper (22) and gold (23) are deposited to provide desired electrical contact to the aluminum lands (18). Chromium deposit (21) establishes an excellent glass to metal seal and ensures environmental protection of the contact area. The copper (22) and gold (23) deposits permit metals to be adhered to chromium sealing film (21). From the teachings of Merrin and Yabe, we conclude that it would have been obvious to one of ordinary skill in the art to have provided the bump electrode (4) of Yabe with a metal layer in contact with the bump electrode as taught by Merrin. One of ordinary skill in the art would have been taught to make this modification because the chromium layer would provide a better contact between the SiO_2 powder in the polyimide layer (5) and the bump electrode (4). In addition, the copper and gold deposits on the chromium layer would provide a better electrical contact with the bump electrode. In providing a metal layer around the bump electrode (4) of Yabe, the metal layer would be in contact with the aluminum layer on which the electrode is placed.

Appellants further assert that the references do not disclose or suggest the claimed bump electrode projection distance. The examiner takes the position (answer, page 3) that "resin film (5) has a thickness of +0 to -10 microns in [sic: with] respect to the height of the bump electrode." Appellants' position (reply brief, page 6) is that although Yabe discloses film having a thickness of +0 to -10µm with respect to the height of the bump electrode, the reference lacks any mention of projecting a bump electrode above a top surface of the resin film to reduce heat induced defects and absorb pressure. Claims 17 and 21 require that the bump electrode project a distance above a top surface of the resin film, with the projection distance reducing heat induced defects and absorbing pressure exerted on a top area of a bump electrode to suppress the occurrence of cracks in the resin film. Yabe's invention is directed to (translation, pages 2 and 3) the structure of a protective film on the surface of a semiconductor device which is mounted by a TAB format. Yabe states (translation, page 3) that conventionally, surface protective film structures involve forming a thin, 2-5µm polyimide film over the whole surface of a semiconductor chip. According to Yabe, the drawback of this construction is that the surface protective film is too thin. As a result, the TAB lead and the chip end come into contact, and shorting occurs. To resolve this problem, Yabe makes the polyimide first surface protective film (5) 18µm in thickness (translation, page 4). In addition, Yabe (translation, page 4) provides the polyimide film (5) at a thickness of +0 ~ -10 µm relative to the height of the bump electrode (4). As Yabe teaches making the the polyimide film (5) at a thickness of +0 ~ -10 µm relative to the height of

the bump electrode (4) to prevent shorting of the connection between a TAB lead (7) and the bump electrode (4), we conclude that Yabe fairly suggests forming the bump electrode at a projection distance above the polyimide film (5) that will ensure a proper connection between the TAB lead and the bump electrode (4). Appellants assert that Yabe lacks disclosure of reducing heat induced defects or absorbing pressure to suppress occurrence of cracks in the resin, and cites (reply brief, page 7) ***In re Dillon***, 919 F.2d 688, 693, 16 USPQ2d 1897, 1901 (Fed. Cir. 1990) (***en banc***), ***cert. denied***, ***Dillon v. Manbeck***, 111 S.Ct. 1682 (1991) asserting that "[i]n an obviousness analysis, the properties of a claimed invention and the prior art must be considered in determining the ultimate question of patentability." We find that both Yabe and appellants are concerned with providing a connection between the bump electrode of a semiconductor device and a bonded lead. Both Yabe and appellants achieve the connection by providing a bump electrode over a semiconductor substrate to allow signals to be input to and output from a semiconductor device and a resin film on a surface of the semiconductor substrate except at the top area of the bump electrode (specification, page 2 and Yabe, translation, pages 3-5). In appellants' invention, the bump electrode projects a distance above the top surface of the resin film (6). In Yabe, the polyimide film (5) has a thickness of +0 ~ -10μm with respect to the height of the bump electrode (4). While appellants project the bump electrode above the resin film to reduce heat defects and absorb pressure during the bonding process, Yabe sets the thickness of the polyimide film with respect to both overall thickness of 18μm and between +0 ~ -10μm with respect

to the height of the bump electrode to prevent the short circuit that occurs during the manufacturing process if the TAB lead and chip come into contact. While Yabe's reasons for setting the thickness of the resin film with respect to the height of the bump electrode are not identical to those of appellant, Yabe achieves the same results as appellants as Yabe sets forth that the polyimide film (5) has a thickness of +0 ~ -10 μm with respect to the height of the bump electrode. Moreover, we note firstly, that as a general proposition, as long as some suggestion to combine the teachings of the references is provided by the prior art as a whole, the law does not require that the references be combined for the identical reasons contemplated by the inventor. ***See In re Dillon***, ***id.*** at 1901. Secondly, we note that we are not relying upon Yabe's teachings of resin film thickness with respect to the height of the bump electrode as a basis for combining the teachings of Yabe with the other references, as the other references to Merrin and Engeler are relied upon in the rejection for different issues.

The examiner also relies upon Engeler for a teaching that the metal layer contains Pd, Ni and Ti. However, we note that independent claims 17 and 21 do not contain this limitation. We therefore consider this reference to be surplusage with respect to the rejection of claims 17 and 21. Accordingly, the rejection of claims 17 and 21 under 35 U.S.C. § 103 as being unpatentable over Yabe in view of Merrin and Engeler is affirmed[2].

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[2] Even though we sustain the examiner's rejection of claims 8, 17, 18, 21 and 22 under 35 U.S.C. § 103 for additional reasons than that advanced by the examiner, our position is still based on the collective teachings of the references applied in the examiner's answer, and does not constitute a new ground of rejection. ***See In re Bush***, 296 F.2d 491, 496, 131 USPQ 263, 267 (CCPA 1961); ***See In re Boyer***, 363 F.2d 455, 458 n.2, 150 USPQ 441, 444 n.2 (CCPA

Turning now to claim 8, which depends from claim independent claim 17, and claims 18 and 22 which depend from claims 17 and 21, respectively, as appellants have not specifically argued the limitations of these claims, the rejection of claims 8, 18 and 22 under 35 U.S.C. § 103 is also affirmed.

Turning now to claims 9 and 19 which depend from claim 17, and claim 23 which depends from claim 21, appellants assert that the references do not suggest that the thickness of the resin film (6) is within a range of 4-5μm (claim 9), or about 4-5μm (claims 19 and 23). The examiner's position (answer, page 3) is that it would have been an obvious matter of design choice as a mere change in size of a component. Appellants' position (reply brief, pages 10 and 11) is that the references "lack disclosure or suggestion of the recited resin film and its thickness. Even if film 5 disclosed in Yabe could be considered hypothetically to be resin film, there is no suggestion or motivation for modifying film 5 to have a thickness such as that recited" [1st and 3rd emphasis added]. At the outset, we note that appellants disclose film (6) to be a "polyimide resin" (specification, page 11). In Yabe (translation, pages 2, 4 and 5) the first surface protection film (5) is a "polyimide film" which we find to be a "resin film" as is appellants' film (6).

Turning to the issue of the 4-5 μm thickness of the resin film (6), as stated ***supra***, Yabe discloses (translation, page 2) that conventionally, the polyimide film was 2-5μm in thickness, but that this led to shorting due to the TAB lead and the chip end coming into contact. Yabe's improvement

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1966).

includes making the film (5) 18μm in thickness. However, even thoughYabe teaches away from utilizing a polyimide film that is 2-5 μm in thickness, Yabe nevertheless establishes that it would have been obvious to have made the polyimide layer about 4-5μm in thickness. While it may be a step backward in the art, it still would have been well within the level of skill to one of ordinary skill in the art as disclosed by Yabe. Accordingly, the rejection of claims 9, 19 and 23 under 35 U.S.C. § 103 is also affirmed.

Turning now to independent claims 16 and 26, these claims are similar to claims 17 and 21 and additionally require, ***inter alia***, a passivation film covering a surface of the semiconductor substrate and a surface of the electrode pad. Additionally, claim 16 calls for the resin film (6) to cover a surface of the semiconductor substrate (1) except at a top area of the bump electrode (5a). Claim 26 additionally calls for the resin film to be disposed on the passivation film (3) and having an opening positioned above the opening of the passivation film. Appellants' position is that film (6) of Yabe is not disposed on an electrode pad, and that in Merrin, even if glass layer (19) were considered to be a passivation film and to be disposed on a semiconductor substrate, that there is no suggestion or motivation for combining with Yabe. We find that in Yabe, second surface protection film (6), composed of silicon nitride or SiO_2, is a passivation layer located on the semiconductor substrate except in the area surrounding the bump electrode (4) and the edge of the chip (1). In Yabe, as stated ***supra***, the polyimide first surface protection film (5) surrounds chip (1) and includes powdered SiO_2 around the bump electrode (4) to

provide moisture resistance. In Merrin, we find that the glass layer (19) to be a passivation layer. We note that appellants' passivation film (3) can be formed of phosphosilicate glass (specification, page 6 and claim 16). Because Yabe does not extend the polyimide film (6) into the area of the bump electrode (4), but instead uses powdered SiO_2 in the polyimide film (5) around the bump electrode (4), we conclude that it would have been contrary to Yabe's teachings to extend the surface protection film (6) into the area of the bump electrode (4). We further conclude that there would have been no suggestion to have polyimide film (6) of Yabe extend below passivation film (5) in view of Yabe's teaching of having each of the protective layers cover separate areas of the semiconductor chip (1), and in view of Merrin's' teaching of having only a single protective layer (19).

The examiner also relies on the reference to Engeler for a teaching of the metal layer containing Pd, Ni and Ti. We note that while this limitation does not appear in claim 26, this limitation is recited in claim 16. Appellants do not present any arguments regarding this limitation. We therefore find that Engeler teaches forming a metal layer in a semiconductor connection from Pd, Ni and Ti (col. 2, lines 44-51) and conclude that Engeler would have fairly suggested utilizing Pd, Ni and Ti for the metal layer. Claim 16 also requires that the metal layer has a thickness of about 4000 angstroms, i.e., .4µm. We find that Engeler is silent as to the thickness of the metal layer, as is Merrin. Appellants' position is that the references do not disclose or suggest the 4000 angstrom thickness of the metal layer (4a). The examiner's answer is silent as to this limitation. However, we need not reach this issue as Engeler does

not overcome the deficiencies of Yabe and Merrin with respect to the claimed limitations regarding the passivation layer, as set forth, ***supra***.

Accordingly, we will reverse the rejection of claims 16 and 26 under 35 U.S.C. § 103. As claims 11-15, 27 and 28 depend from claim 26, the rejection of these claims on the same grounds as claim 26, is also reversed.

Turning now to claims 20 and 24, which depend from claims 17 and 21, respectively, these claims contain limitations similar to those of claims 16 and 26 as claims 20 and 24 additionally recite a passivation layer disposed on the surface of the semiconductor substrate and on a surface of the electrode pad. Accordingly, the rejection of claims 20 and 24 under 35 U.S.C. § 103 is reversed for the same reasons as the rejection of claims 16 and 26.

Turning now to the rejection of claim 25, appellants assert that the references do not disclose or suggest a film carrier tape (11) of a resin substantially the same as a resin of the resin film (6). The examiner's position is that as shown in figure 8 of appellants' disclosure, the carrier tape claimed is the same as the TAB (tape adhesive bonding) of Yabe. We find that while Yabe discloses TAB lead 7, and that TAB lead 7 will attach to a carrier tape, Yabe does not disclose a disclose a film carrier tape formed of a resin substantially the same as a resin of the resin film (6). Appellants' disclose (specification, page 10) that:

> Since the polyimide resin film 6 and film carrier tape 11 are made of the same-based resin, a better heat resistance cycle property can be obtained in a semiconductor

> device. To be specific, the thermal expansion coefficient of the tape 11 and that of the resin film (surface protective film) 6 become substantially the same and, even if the tape 11 is repeatedly expanded and contracted, the resin film 6 is correspondingly expanded and contracted in repeated fashion.

The examiner's unsupported statement (answer, page 6) that there is nothing patentably distinguishable between appellants' carrier tape and Yabe's TAB is insufficient to meet the examiner's burden of producing a factual basis for the rejection.

We are not inclined to dispense with proof by evidence when the proposition at issue is not supported by a teaching in a prior art reference or shown to be common knowledge of unquestionable demonstration. Our reviewing court requires this evidence in order to establish a ***prima facie*** case. ***In re Piasecki***, 745 F.2d 1468, 1471-72, 223 USPQ 785, 787-88 (Fed. Cir. 1984); ***In re Knapp-Monarch Co.***, 296 F.2d 230, 232, 132 USPQ 6, 8 (CCPA 1961); ***In re Cofer***, 354 F.2d 664, 668, 148 USPQ 268, 271-72 (CCPA 1966). Our reviewing court states in ***In re Piasecki***, 745 F.2d 1468, 223 USPQ 785, 788 (Fed. Cir. 1984) the following:

> The Supreme Court in ***Graham v. John Deere Co.***, 383 U.S. 1 (1966), focused on the procedural and evidentiary processes in reaching a conclusion under Section 103. As adapted to ex parte procedure, Graham is interpreted as continuing to place the "burden of proof on the Patent Office which requires it to produce the factual basis for its rejection of an application under section 102 and 103." ***Citing In re Warner***, 379 F.2d 1011, 1020, 154 USPQ 173, 177 (CCPA 1967).

We find that neither Yabe, nor either of Merrin or Engeler discloses or suggests a film carrier tape formed of a resin substantially the same as a resin of the resin film. Accordingly, the rejection of claim 25 under 35 U.S.C. § 103 is also reversed.

In closing, we draw attention to the statement made by appellants' (reply brief, page 3) that "[a]ppellants disagree with the 35 U.S.C. § 103 rejection of claims 8, 9, and 11-28. For at least the following reasons, the board should reverse this rejection" [emphasis added]. As stated by our reviewing court ***In re Baxter Travenol Labs.,*** 952 F.2d 388, 391, 21 USPQ2d 1281, 1285 (Fed. Cir. 1991), "[i]t is not the function of this court to examine the claims in greater detail than argued by an appellant, looking for nonobvious distinctions over the prior art."

37 CFR § 1.192(a)(July 1, 1996) ***as amended at*** 60 Fed. Reg. 14518 (March 17, 1995), which was controlling at the time of appellants filing the brief, states as follows:

> The brief . . . must set forth the authorities and arguments on which the appellant will rely to maintain the appeal. Any arguments or authorities not included in the brief may be refused consideration by the Board of Patent Appeals and Interferences, unless good cause is shown.

Also, 37 CFR § 1.192(c)(8)(iv) states:

> For each rejection under 35 U.S.C. 103, the argument shall specify the errors in the rejection and, if appropriate, the specific limitations in the rejected claims which are not described in the prior art relied on in the rejection, and shall explain how such limitations render the claimed subject matter unobvious over the prior art. If the rejection is based upon a combination of references, the argument shall explain why the references, taken as a whole, do not suggest the claimed subject

> matter, and shall include, as may be appropriate, an explanation of why features disclosed in one reference may not properly be combined with features disclosed in another reference. A general argument that all the limitations are not described in a single reference does not satisfy the requirements of this paragraph.

Thus, 37 CFR § 1.192 provides that this Board is not under any greater burden than the court which is not under any burden to raise and/or consider such issues. Therefore, we are not required to raise and/or consider such issues.

SUMMARY

The rejection of claims 8, 9, 17-19 and 21-23 under 35 U.S.C. § 103 is affirmed. The rejection of claims 11-16, 20 and 24-28 under 35 U.S.C. § 103 is reversed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED-IN-PART.

KENNETH W. HAIRSTON Administrative Patent Judge	)	
MICHAEL R. FLEMING Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES
STUART S. LEVY Administrative Patent Judge	)	

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